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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,318	07/10/2003	Thomas David Zounes	02-LJ-060	1317

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STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
PERALTA, GINETTE	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/604,318	ZOUNES, THOMAS DAVID	
	Examiner	Art Unit	
	Ginette Peralta	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *34-37* is/are withdrawn from consideration.

5)☒ Claim(s) *1-26* is/are allowed.

6)☒ Claim(s) *27-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-33 in the reply filed on 11/3/04 is acknowledged.

2. Claims 34-37 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 11/3/04.

Drawings

3. The drawings were received on 4/27/05. These drawings are accepted by the Examiner.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 27-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Essbaum et al. (U. S. Pat. 5,814,846).

Regarding claim 27, Essbaum et al. discloses in Fig. 2 a cell library that comprises a plurality of selectable inverting NMOS logic circuits (item 34 of Fig. 1, col. 3, lines 59-61, and in col. 4, lines 58-63); and a plurality of selectable inverter circuits (item 18 of Fig. 1), connectable to receive at least one output from a selected NMOS logic circuit to provide at least selectable transistor sizes (as disclosed in col. 3, lines 54-67 where the components have certain size ratios that correspond between the elements.

Regarding claim 28, Essbaum et al. discloses a cell library wherein at least one of the inverter circuits 18 has a plurality of inputs to which outputs of a corresponding plurality of the logic circuits 34 are selectively connectable, as shown in Fig. 1.

Regarding claim 29, Essbaum et al. discloses that at least one of the NMOS logic circuits has an "AND" function in col. 3, lines 59-61.

Regarding claim 30, Essbaum et al. discloses that at least one of the NMOS logic circuits has an "OR" function in col. 3, lines 59-61.

Regarding claim 31, Essbaum et al. discloses that at least one of the NMOS logic circuits has a complex logic function including "AO" (AND/OR) or "OA" (OR/AND) functions in col. 3, lines 59-61.

Regarding claim 32, Essbaum et al. discloses that a weak p-feedback transistor may be added to the circuit at the inverter region as shown in Fig. 1, and this would result in the inverter circuit being configured as a keeper circuit that is connected to the NMOS logic circuit 34.

Regarding claim 33, Essbaum et al. discloses that the keeper circuit comprises a pair of PMOS devices (items 16 and 20 of Fig. 1) and an NMOS device (item 22 of Fig. 1); the NMOS device 22 and one of the PMOS devices (20) being connected to form an inverter circuit connectable to an output of the NMOS logic circuit 34; and another of the PMOS devices (16) being connected to receive an output of the inverter circuit and connectable to the output of the NMOS logic circuit 34 to latch an existing state therein (col. 4, lines 17-23)

Allowable Subject Matter

6. Claims 1-26 are allowed.

The primary reason for the allowance of the claims 1-15 is the inclusion of the feature of a cell library for use in designing integrated domino logic circuits that comprises a first library portion including a plurality of FET logic circuits to provide at least selectable transistor sizes, and a second library portion that includes a plurality of selectable prechargeable complementary FET driver circuits, each configured to be connectable to an output of the selected logic circuit, to provide at least selectable transistor sizes which is not anticipated nor rendered obvious over the prior art hereby made of record.

The primary reason for the allowance of the claims 16-26 is the inclusion of the feature of a cell library for use in designing integrated circuits that comprises a first library portion including a plurality of NMOS logic circuits to provide selectable logic functions and transistor sizes, and a second library portion that includes a plurality of

selectable driver circuits, each configured to be connectable to an output of the selected logic circuit, the driver circuit selectable to match at least the size characteristic of the selected logic circuit which is not anticipated nor rendered obvious over the prior art of record

The prior art includes Kawabe et al. (US Pat. Pub. 2002/0099989 A1), which discloses a cell library for use in designing logic circuits, and that includes determining the leakage current of a determined circuit and assigning the cell depending the input signals generated as determined by the leakage current, but does not disclose a first portion having a plurality of FET logic circuit with a selectable size, and a second portion including a prechargeable complementary FET driver circuit that provides selectable transistor sizes. The prior art further includes Chen (U. S. Pat. 6,711,720 B2), which discloses a library of gates that are selectable based on their size to be used in logic circuits in order to optimize the power dissipation and the circuit speed of the integrated circuit.

Response to Arguments

7. Applicant's arguments filed 4/27/05 have been fully considered but they are not persuasive.

Regarding the inclusion of the phrase "to provide at least selectable transistor sizes" in claim 27, it is noted that Essbaum et al. discloses that the cells selected from the library to from a certain circuit includes providing transistors of different sizes as disclosed in col. 3, lines 54-67. Thus, the claim is still anticipated by Essbaum et al.. It is

further noted that this feature in combination with the other features in the claims is what makes claims 1-26 allowable and not the feature by itself..

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,785,875 B2	Beerel et al.	8/31/04
US 2002/0144223 A1	Usami et al.	10/3/02

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571) 272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GP

Wael Fahmy
SPE 2814